**Replacement Claims**

59. (Twice Amended) A integrated circuit substrate, comprising:

a substrate;

an oxide layer formed over said substrate; and

a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes, said reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma.

92. (Amended) A integrated circuit substrate, comprising:

a substrate;

an oxide layer formed over said substrate; and

a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a decreased critical dimension loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma.